As the semiconductor industry shifts from 200- to 300-mm wafers, the use of ozonated deionized water (DIO3) in surface cleaning processes is expected to become common. The technology, which has the potential to lower operating costs while maintaining process capabilities, has been widely studied, with particular emphasis on its application in photoresist removal after dry etching or ion implantation.1-6

Most photoresist removal procedures consist of a combination of plasma-induced dry ashing and wet chemical treatments. Problems associated with the dry ashing process include incomplete resist removal and undesired by-products caused by the reaction among the photoresist, oxidizing gas, and dry etch residue. However, an even greater concern is the undesirable effects on electrical properties, such as intrinsic total charge to breakdown (QBD) and electrical breakdown fields, that can be caused by plasma-induced damage to sub-0.18-µm devices with a gate oxide of <40 Å. In addition, the oxidation reaction that occurs between the etch residue and the oxidizer gas in the plasma chamber during dry ashing creates residue that is difficult to remove in subsequent wet cleans.

Traditional wet cleaning processes rely on a mixture of sulfuric acid and hydrogen peroxide (SPM) or sulfuric acid with ozone (SOM). Although these chemicals are highly effective, the operating costs for sulfuric-based processes are significant.7 Vast amounts of DI water are consumed to rinse off residual sulfuric acid and unoxidized particulate matter from wafer and carrier surfaces during the wet cleaning process, and expenses are incurred both in obtaining the water and treating and disposing of postprocess wastewater. Other operating costs include the expenses involved in the storage, distribution, and treatment of sulfuric acid mixtures and in the frequent replacement of wet station components. Such components have limited life spans because of their...
constant exposure to high process temperatures—generally >130°C—and the corrosive properties of the acid. The use of a DIO₃ cleaning tool, such as that developed by Akrion (Allentown, PA), can offer several advantages over other photoresist removal procedures. Its adoption can simplify the stripping process by replacing two separate steps—dry ashing and wet cleaning—with one, and reduce operating costs by eliminating expensive, and environmentally unfriendly, sulfur-containing process chemicals. While minimizing defect densities and organic residue, the technology may also offer a smaller footprint than methods that require multiple process baths.

**The DIO₃ Process**

Unlike the SPM process, in which resist is undercut, floats away, and then is oxidized by hydrogen peroxide, the DIO₃ process directly oxidizes resist on the wafer surface. The resist becomes progressively thinner during this reaction, and the cleaning solution remains clear during the entire process. The chemical reaction that takes place during the DIO₃ process is

\[-\text{CH}_2^- + 3\text{O}_3 \rightarrow 3\text{O}_2 + \text{CO}_2 + \text{H}_2\text{O}\]

and the reactions in SPM processes are

\[\text{H}_2\text{SO}_4 + \text{H}_2\text{O} \rightarrow \text{H}_2\text{SO}_5 + \text{H}_2\text{O}\]

\[-\text{CH}_2 + 3\text{H}_2\text{SO}_5 \rightarrow 3\text{H}_2\text{SO}_4 + \text{CO}_2 + \text{H}_2\text{O}\]

Figure 1 depicts the two types of stripping procedures in simplified schematic drawings. In addition to directly oxidizing the resist, the oxidation reaction in DIO₃ processing between ozonated water and bare silicon induces the growth of a thin (~9.5-Å) oxide layer on the wafer surface. This chemically induced oxide minimizes particle additions because both the zeta potential on the silicon surface and the Van der Waals attractive force between the wafer and particles are reduced when the previously hydrophobic surface is rendered hydrophilic. The oxidation reaction also minimizes levels of total organic compounds.

The flow scheme in the DIO₃ immersion equipment is shown in Figure 2. In this system, ozone is produced from O₂ gas in an ozone generator and fed into a static mixer, where it is combined with DI water. This mixture is then fed into the bottom of the process bath. Gaseous ozone is also fed in a uniform stream to the bottom of the process bath via a specially designed diffusion device. The gaseous and dissolved ozone enter the bath simultaneously, and both are monitored using in-line analysis. With closed-loop recirculation, liquid flows from the process vessel to a pump, after which it flows through a heat exchanger, a sensor, and a filter back to the mixer. Finally it reenters the vessel. In this system, the dissolved ozone concentration stabilizes in the range of 10–50 ppm, depending on the process temperature (which can range from 18° to 50°C).

**Process Optimization Studies**

During the development of the DIO₃ system, a variety of tests were conducted to assess the technology’s photoreist removal effectiveness.

**Strip Rate.** One set of tests assessed the effect of process temperature and ozone concentration on the average photoreist stripping rate. As the results in Figure 3 indicate, the stripping rate increased dramatically with an increase in the dissolved ozone concentration in the process bath. The data also show that the optimal baked-photoreist removal rate averaged 65 nm/min at ambient temperatures <40°C. This low-temperature capability greatly simplified equipment design and maintenance by eliminating the need for an upstream heater or heat exchanger. Strip-rate tests were run using many types of photoreist in addition to that used to achieve the results shown in Figure 3. The resists tested included AZ 1518, 7209, and 7220; HIPR 512; JSR 7158 and IX710; MCPRi 7010; PFX 15D1; PFI 26A, 26B, and 38A9; Shipley S1808 and S1813; and System 827.
THMR-ip 3300. It was found that the stripping rate does not depend on the resist type.

Although the removal rate achieved in this testing seems low compared to some previously published data from studies at subambient temperatures, it should not be a concern in future device manufacturing processes. The photoresist thickness used in critical processes such as gate line, deep and small metal contact, and shallow trench isolation is expected to remain below 500 nm for sub-quarter-micron IC devices.

**Microcontamination.** In implementing the DIO₃ technology, the level of metal contaminants in the process bath was a major concern for several reasons. The process tool uses a metallic electrode to generate reactive ozone from oxygen, and it is known that metallic impurities have a tendency to adhere to hydrophobic surfaces after photoresist stripping. Minute amounts of such impurities can cause various defects, including silicide/silicate formation, gate oxide integrity failure, silicon surface pitting, and electrical current leakage in dielectrics in front-end processes. To address this concern, the metallic contamination contribution of the DIO₃ process was evaluated using vapor-phase decomposition total reflection x-ray fluorescence spectroscopy (VPD-TXRF). Comparative results for wafers processed by either DIO₃ or
SPM are presented in Table I. As these data indicate, no significant metallic contamination was observed on wafers processed with DIO3. In addition, sulfur contamination, a significant cause of wafer surface hazing associated with SPM processing, was not observed following the ozonated-water process. It is believed that DIO3 eliminates ionized metallic impurities from the wafer surface via the oxidation reaction of the highly reactive ozone radical (O$_3^+$).

<table>
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<tr>
<th>Process Type</th>
<th>Metallic Contaminant ($10^{10}$ atoms/cm$^2$)</th>
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<tr>
<td></td>
<td>S</td>
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<tr>
<td>SPM</td>
<td>750</td>
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<tr>
<td>DIO$_3$</td>
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<tr>
<td>Reference wafer (unprocessed)</td>
<td>82</td>
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<tr>
<td>Detection limit (DL)</td>
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Table I: Metallic contamination levels measured using VPD-TXRF on a reference wafer and following resist stripping with either an SPM or DIO$_3$ technology. The measurement instrument’s detection levels for each metal are also listed.

The stripping rate increased dramatically with an increase in the dissolved ozone concentration in the DIO$_3$ process bath.

In a typical manufacturing environment, the SPM photoresist stripping process sequence includes RCA standard cleans 1 and 2 (SC-1 and SC-2). The SC-2 clean, which consists of hydrochloric acid (HCl) and hydrogen peroxide, is used to remove metallic residues such as iron and zinc, which are often deposited during the SC-1 step. With DIO$_3$ processing, injecting a small amount of HCl into the process water or the postprocess rinsewater effectively removes such trace metals from the wafer surface, eliminating the need for the SC-2 step and thereby lowering overall operating costs.

The possibility of eliminating the SC-1 step following the DIO$_3$ process was also investigated. In that study, surface particles ≥0.16 µm were measured with a Surfscan 6200 (KLA-Tencor, San Jose). As shown in Table II, the final particle counts following a DIO$_3$/SC-1/rinse/dry sequence were lower than those obtained following DIO$_3$/rinse/dry or DIO$_3$/dry sequences. Compared to the DIO$_3$/rinse/dry results, the counts were approximately 25% lower when the SC-1 step was included.

On certain highly implanted wafers, where the photoresist is used as a blocking layer to form a shallow junction (for source and drain) after gate etch, it is desirable to combine dry ash and wet chemical stripping processes. In such cases, SPM followed by SC-1 is the usual post-dry-ashing wafer cleaning sequence. The role of SPM is to remove by-products that are formed during the reaction between metallic impurities from the wafer surface via the oxidation reaction of the highly reactive ozone radical (O$_3^+$).

### Table II: Total particle counts at ≥0.16 µm on unashed wafer surfaces following various DIO$_3$ process sequences.

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photoresist and the reactive gas in the ashing chamber. To investigate the use of ozonated water rather than SPM in this postash cleaning step, light-point defect measurements were taken on wafers that had been treated using various process sequences. As shown in Figure 4, the DIO3-only treatment was not sufficient to obtain good defect counts; however, the combined DIO3 and SC-1 process sequences yielded satisfactory to excellent results, particularly when a 20-minute DIO3 immersion was used.

The Recommended Process. Based on the studies discussed above and assuming a common device structure of <12,000 Å, the recommended process sequence for photoresist removal with DIO3 is as follows:

1. A 15–20-minute immersion in the DIO3 process bath at ambient temperature to remove photoresist.
2. SC-1 processing for 7–10 minutes at 50°C with megasonic to remove particles and light organics.
3. A 7–10-minute cascade-type DI rinse at ambient temperature to rinse off the SC-1 chemistry and cool the wafers.
4. An 8.5-minute cycle in a dryer to remove rinsewater from the wafers.

As the micrographs in Figure 5 indicate, this DIO3/SC-1/rinse/dry sequence thoroughly removes the photoresist from a patterned wafer. (Before undergoing the DIO3 process, the wafer shown had a 1.05-µm thick HipR 6512 resist layer hard baked at 100°C.)

Electrical Performance and Yield

In another study (the results of which are presented in Figure 6), researchers investigated the effect of DIO3 processing on device properties and yield. In that work, the intrinsic breakdown of thin oxide on simple gate modules was measured on wafers cleaned with either a DIO3 or SPM process followed by standard cleans SC-1 and SC-2. The gate oxide layer was 120 Å thick. These measurements indicated that the probability of intrinsic QBD failure—which may result from defects caused by such contaminants as particles, organic residue, and metallic impurities—did not differ significantly for wafers cleaned with the two processes. Yield loss for wafers processed using DIO3 was also comparable to that for wafers cleaned with SPM.

Conclusion

Studies have shown that DIO3 is a viable substitute for sulfuric acid mixtures in semiconductor resist stripping processes. When followed by an SC-1 clean, DIO3 processing minimizes metallic contamination and particle addition on the wafer surface. The technology is also environmentally friendly and reduces operating costs because it eliminates the use of corrosive chemicals. More importantly, neither electrical device characteristics nor overall production yields are negatively affected by using the DIO3 process.

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References


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